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Design of the Signal Lamp Board Tester for Object Controller System in Rail Transport Based on Hardware in the Loop Simulation

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A B S T R A C T

The hardware in the loop simulation has many uses in design, calibration, and performance validation of initial prototypes made from controllers. Using this feature, the reliability and time of commercialization required by the system with an effective cost method can be maintained. Considering the importance and cost of object controller system in the rail transport, the use of hardware in the loop in the development of these controllers at all stages of design and implementation can be a significant useful aid. In this article, a hardware in the loop test-table is designed and used for testing the performance of the objective controller's Lamp board, known as controller and communication display board. In this regard, the simulator's performance is evaluated after assurance of its proper functioning by an accuracy test. The design table consists of a host computer, RS232 data transmission, and the Arduino board. The results show that the designed test table can be used to evaluate the accuracy or inaccuracy of all the algorithms used without the cost of testing on the actual system due to a real-time communication. The length of the development of the board is reduced greatly by this method.

1. Introduction

The equipment known as the object controller (OC) actually provides a link between the interlocking system and wayside equipment, including point machines, signaling, and axle-counter systems. OCs are located in the predefined areas along the line. Each OC includes common components that make installing, commissioning and maintenance more efficient due to standardization of parts. Since this system has a very important position in the rail transport industry, the design of its successful installation leads to lower costs in each stage. Due to the high sensitivity and cost of repairing and re-designing, as well as preventing damage to line equipment and interlocking systems, it is needed to ensure their performance before installation. How to test control systems is a matter of importance.

Hardware in the loop (HIL) simulation allows validation tests of control systems in a short time, safe and cost-effective environment by creating a virtual model for the environment around a hardware system and establishing a relationship between them. Aurelio and Sanvido [1] presented the uses of the HIL process in simulation framework. Its sparks flooded in the air industry, and today it is used in all industries. One of the control systems in the transportation is the traffic control system, which is usually difficult, unmanageable and time-consuming. Field studies of traffic control strategies versus microscopic traffic simulation are less studied. Sullia [2] provided HIL simulation for development and evaluation of traffic signal optimization with the traffic

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controller capacity in the microscopic simulator known as a HIL simulation. It provides a laboratory environment to evaluate the systems' function. On the other hand, Automatic Train Protection System (ATP) also plays a significant role in controlling traffic of rail transport system. ATP system minimizes the speed of a train, or stops the train if a train passes beyond an authorized range. The Oudometric algorithm is a sub-system of ATP to estimate the train speed and position. The accuracy of Oudometric estimates has a great influence on the ATP behavior. Therefore, it must be designed and verified with care and diligence. Addeo et al. [3] developed a HIL simulator to test the Oudometric system used in ATPs in the Italian Railways Fleet called SCMT.

Mayet et al. [4] declared that Multi-train systems have their own complexity due to the size and characteristics of the system. To study such networks, HIL simulation used a single train first and expanded for two trains to analyze flow of different powers between sub-systems. In addition, the HIL simulator can be used to analyze the error of various systems, such as traction system and train braking force in adhesion conditions. Del Olmo et al. [5] provided a model driven HIL fault analysis of railway traction systems. For this purpose, Allotta et al. [6] applied a HIL railway roller rig model for the traction and braking testing activities under degraded adhesion conditions. Conti et al. [7] developed a HIL simulation for the braking system under adhesion condition. To investigate the trains' brake system, Lee et al. [8] evaluated the hysteresis function and the dynamics of the pneumatic cylinder in the HIL. The suspension system included active or semi-active technology.

The use of these systems in a real vehicle is not easy due to cost and time. Therefore, Kwak et al. [9] used the HIL simulation for validation of this system. Bolandi et al. [10] presented a practical solution to achieve a fault tolerant attitude control system capable of Fault Detection and Diagnosis. Through extensive simulation results, the designed algorithms are shown to be robust and accurate. Also, designed algorithms are assessed through hardware in the loop test bed to evaluate their functions in a experimental situation. Maleki et al. [11] proposed two maximum likelihood estimators to estimate the real time of step changes and drift in Phase II monitoring of binary profiles in the case of within-profile autocorrelation, respectively. Rezaee and Zamani [12] proposed a new method for automatic generation of test cases using model based testing. As test model, class and state diagrams were used, and constraints were expressed using OCL. The tool shows good result in terms of test case generation execution time, test goals satisfaction rate, source code instructions coverage, and also boundary values generation. The HIL simulation is the one state of model based design (MBD). Manfred [13] explained about benefit of a model-based design of embedded software systems in the car industry. Hoxha et al. [14] presented a mining parametric temporal logic properties in model-based design for cyber-physical systems. For other controlling systems in the rail transport it can be referred to OC, which plays the role of the interface between the interlocking system and wayside equipment. CReO [15] reports a comparative analysis of the interlocking systems such as OC. Hagelin [16] discusses about the subsystems of OC, their relationship with each other and maintenance of the components. Bombardier Company [17] deployed this system in Pakistan railways rehabilitation signaling project. Puri and Suchit [18] and Teeg and Vlasenko [19] explained that the wayside equipment controlled by OC system includes point machine, signaling and axle-counter.

Therefore, due to the high cost of repairing equipment and preventing damage during launch, HIL can be used to validate the OC system. At present, the Bombardier Company's OCS950 wayside equipment controller system is used in lines 1, 2 and 7 of Tehran subway.

Due to the lack of simulation of OC in previous studies, this research designed, simulated, tested and evaluated the Lamp board (LMP) of this Bombardier system as model in the loop and hardware in the loop. In this regard, real time simulation of the lamp board is achieved by applying a precise model of its performance. The V diagram can be used to determine the types of tests at all stages of design. Mpsterman and Pieter [20] described methods of engineering design based on V diagram. Buede et al. [21] also explained that V diagram expresses all stages of the development, design, and implementation of an embedded system. In general, HIL simulation requires the use of automated code generation. Fraticelli [22] explained a tutorial for generating C code from Simulink models by using Simulink coder.

2. Object Controller System

The OC is a central computer based interlocking (CBI) system, with a system of processor modules that provide a two-way interface between the central interlocking system (CIS) and wayside equipment. The Bombardier OCS 950 system is part of the new generation of the EBI-lock 950 CBI and offers a flexible interface for controlling and monitoring wayside equipment with other common signaling elements. Each OC contains common components, which leads to a more efficient installation, launch, and easier maintenance process due to component standardization [16].

Controlled and supervised equipment on the site can be of vital or non-critical nature, or a combination of both. The most commonly used equipment is the signal (LED or bubble), point machines (up to 16 in a community), the track circuit (AC, DC, frequency and encoded), the axle-counter and ATP equipment, such as balises. One of the key features of the system is its easy compatibility with existing infrastructure. The system is capable of connecting to various types of point machines, interlocking, signaling, track circuit, train detection and ATP equipment. Interfaces for specific applications and wayside equipment can be defined in each case. The system can also monitor and control level-cross intersections, line blocks, relay interlocking systems, I / O interfaces [15]. The OC system duty is receiving and processing commands received from the central interlocking, displaying the status of wayside equipment, sending commands received from interlocking to wayside equipment, and finally sending status information to the CBI system. Through this information and through the OC system, the safety of train traffic is supplied along the line. The basic equipment of the system consists of concentrating loop, concentrating, controlling links, object controller and cable equipment. In Figure 1, the position of each of these components is presented. The CIS system, which controls the logic of interlocking, is placed in a central computer and is connected to a wayside equipment with a number of loops. Each loop considered as a data transmission line, which can include 15 concentrators. The concentrating loop has the ability to communicate with the line bi-directionally to ensure it operates in the event of a cable failure. This feature of the system makes it possible to transfer any data inside the loop.

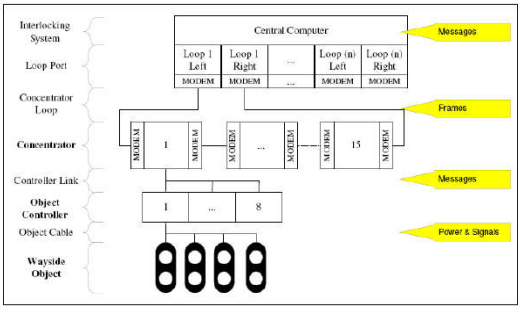

Figure 1. Basic equipment of the OCS950 system

Normally, the CIS system communicates with the concentrators from the front of the loop (left), while monitoring from the secondary (right) side.

Each concentrator is connected to eight Ocs. Each concentrator controls one or more wayside equipment using specific microprocessors. The loop port, which is an open part of the CIS, is connected to the central computer, it deals with the change of information frame, such as message setting and all concentrators in a particular loop, and is dependent on the input and output modules. The concentrator loop generates a moderate data transfer between the loop port and the concentrators. The concentrator acts as the interface between the loop port and the OC, in fact converting the frames from the loop and converting understandable messages to the equipment and vice versa. This section is used in long-distance conditions as a signal amplifier. The data transfer rate in the OCS950 system is 19.2 Kbps [16].

2.1. Sub-Systems of Object Controller

The subsystems of OC, which directly relate to the LMP board performance are described as:

CCM board: In the OC system, the first position on sub-rack belongs to CCM board called the controller and the communication display board. This board is the core of the system processing, which has four inputs for monitoring and detecting the status of critical communication relays, such as the track circuit (occupied, free, out of control), alarm, magnetic key locked point detection and CBI relays and has two non-critical inputs, and six outputs. It is also used as the main board for EEPROM memory for software signaling, software point and software for input and output [17]. The status of the track circuit is transmitted through the relay communication link to the CBI, which acts as a critical input to the CCM. Each OC

offers four dedicated relay communication inputs. Normally, when the line is free, the relay energized, and when the line occupied, it has no energy [23].

LMP board: The LMP board has the task of controlling and monitoring various signals in the line such as the signal of arrival, dispatching, block, shunt, and so on. This board has four modes of proceed output and two outputs of the stop mode. Therefore, if the number of signal light shots exceeds this value, due to the limitation in stop mode display, one should use more LMP board. In an OC system, two LMP boards can be used because of the physical width limit [17]. The input voltage of this board is 110 V for proceed and stop mode, and 28 V for night mode. It should be noted that the frequency and voltage changes of the power supplies are effective in measuring the accuracy of the point flow and the signal light. Therefore, the requirements are such that the input voltage of the power supply should not exceed 10% and the frequency should not be more than 2% oscillation, [16]. In order to connect the signal light to the LMP board, a transformer is used to generate the required voltage. The signal light is connected to the control board outputs. If the OC system is out of control, because of the safety issues, the modes of proceed remain off automatically and the red aspect of the stop mode remains on.

Addressing: In order to address and specify the name and type of equipment that should be illuminated and function properly at the time of execution, hexadecimal binary codes should be used. The object controller addresses are built on the interlocking area, communication loop, concentrator unit (CCU) and object controller. The addressing tool is for generating an address for the OC and CCU, and creating a configuration file for the strap boards (multiple boards in the same sub-rack).

Dipswitches: There are switches called Dip Switch in back plane of the OC system, which are responsible for determining the type of configuration of each OC by four bytes. These switches are located inside the cabinet and behind the control boards, which are accessible from the front door of the cabinet. The first three bytes in this section are determined during the execution of the site map by site engineers, and the fourth byte is obtained through the first three bytes computation [16]. Two sets of Dip switches are available in a sub-rack for each OC. The first being assigned to first position of CCM board and the second belongs to the controller boards associated with this CCM. A schematic for the Dipswitches addressing is presented in Figure 2.

- A1 and A2 Bytes: Specifies the addresses of each OC that are determined by the loop number, CCU, and OC numbers on the hexadecimal basis. Two bytes create a common concept between team members, which can be modified based on the design and type of Interlocking Processor Unit (IPU). The zero bit in A1 is always coded as logic 0 and zero bit in A2 is always coded as logic 1.
- IND byte (Individualization): This byte is used for uniquely addressing. In fact, IND is not used in addressing directly, but it provides information about the configuration of the OC system layout.
- CRC byte: To calculate and evaluate the sub-rack configuration and obtain the redundancy of the system. It is calculated based on A1, A2 and IND.

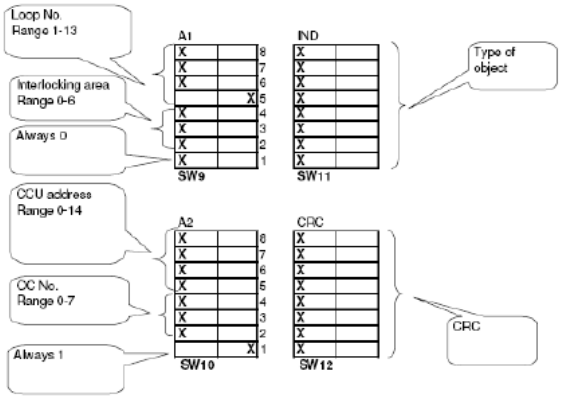

Figure 2. Dipswitches addressing

Strap boards: In the OCS950, the strap board is used to detect the same boards in similar OCs. Straps consist of the address and number of straps. The position and board straps will protect the OC from going in to operation if the wrong boards are used in the wrong position.

3. Real Time Simulation

Implementation of simulation generally involves steps. If these steps coincide with the main events of the system, simulation is in real time. One of the requirements for HIL simulation is the use of real time simulation.

Therefore, it is needed to use a tool that has the ability to simulate in real-time. There are various methods for real time simulations. The most important of these methods are designed under the DOS system, Windows, Real time windows target (RTWT) and XPC-Target tool. Each of these methods has a number of advantages and disadvantages [22]. RTWT simulation technique is used in this project. Two important parameters in real-time simulators are the accuracy of the models and the time step size. These two parameters somehow are balanced in a way that by increasing the accuracy of the models and increasing the details of the modeling, calculation of each step of the simulator becomes more complicated and requires more time for the solution procedures. As a result, increasing the accuracy of the model will increase the time step. Since the time step is the most important parameter during simulation's real time, the models used in these simulators are usually associated with large approximations and little detail. In addition to implement the time step in the implementation of the HIL simulation, two steps of reading information from the input and insertion of the output are also added, all of which should be done in a time step. In the implementation of these steps, problems such as the inability to perform all of the above steps in a certain time occur in some cases.

4. Implementation

The implementation of the selected simulation method is exercised with the signals from a real subway station in Tehran (that is Farhangsara station) that is located along line 2 of Tehran subway tracks. The route map at Farhangsara station has two DW on the right side of the platform output, four SSA and four SSB signal lights at the points are located. The DW single light initially blinks for 5 or 6 seconds, and then until the train has left the platform, it will lit continuously. According to the route map the limit of the number of signal lights can be controlled by a LMP board. The combination of signal of type 4 that is implemented in this section of the track is presented in Figure 3.

In performing the HIL test, it is needed to initially create a list of signals for the system under the examination. It includes all inputs and outputs of the tested system, and includes the range of changes, accuracies, and sampling rates.

The Identification procedures of the input and output signals of the LMP board in the HIL test are presented in Figure 4.

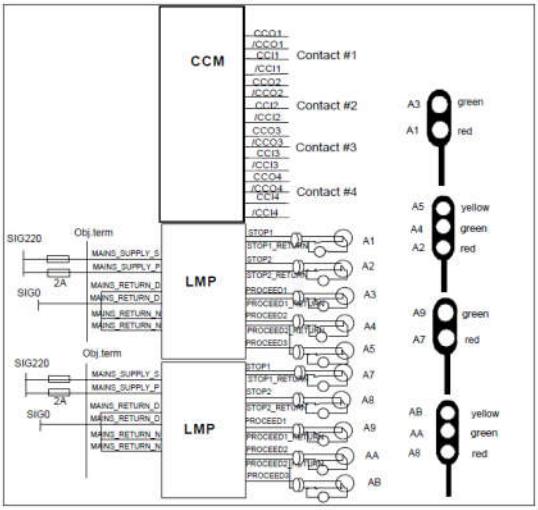

Figure 3. The combination of the signal lights

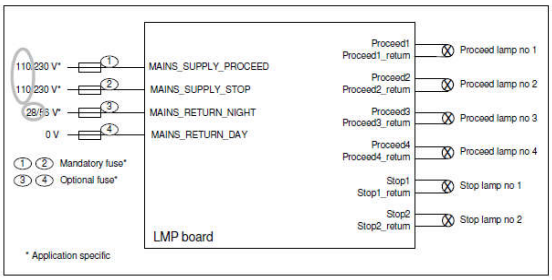

Figure 4. The I/O signals of the LMP board

The characteristic table for setting codes related to type and color of the signal light is according to Table 1. In serial communication, information is considered as a packet of bytes. Since the OCS950 system has a data rate of 19.2 Kbps, the structure of the data packet is according to the schematic in Figure 5. This is to ensure that the data is sent and received correctly.

Table 1. Codes related to type and color of signal

Byte in Decimal	Byte in Binary	Byte in Hex		
64	01000000	40	Green	Color of light
128	10000000	80	Yellow	
192	11000000	C0	Red	
48	00110000	30	White	
255	11111111	FF	On	State of light
0	00000000	0	Off	
252	11111100	FC	SSA	Kind of Signal
227	11100011	E3	SSB	
15	00001111	0F	DW1	
63	00111111	3F	DW2	

Sampling time, sending data and commands to the LMP board from CCM and from LMP to signal lights in this simulation is 0.02 seconds or 50 Hz.

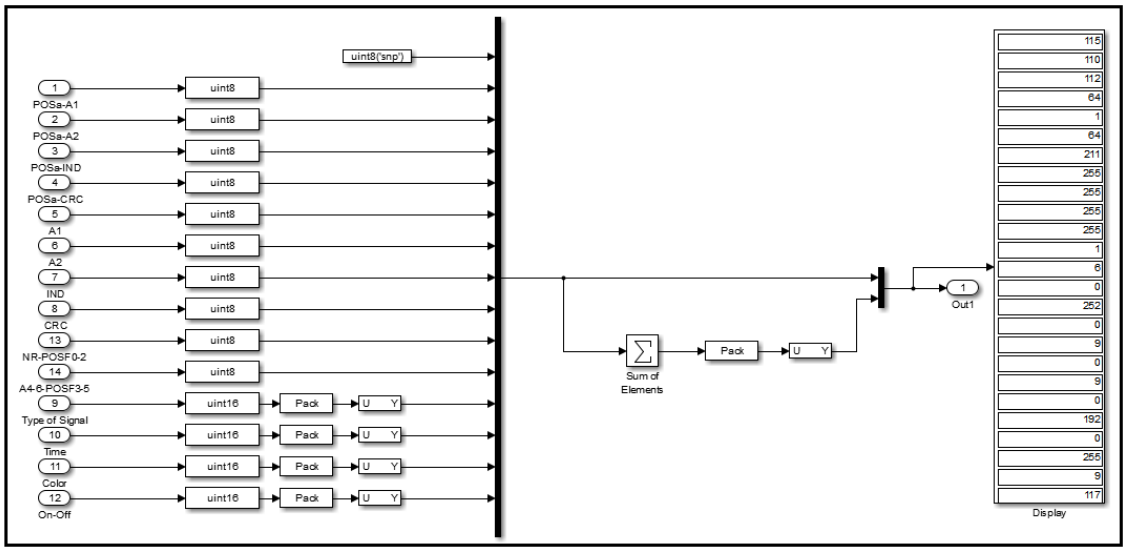

Figure 5. Sending the address and order from interlocking to the OC

In the configuration of the data for each section, addresses and commands are allocated in bytes. After configuring the data, they are sent to any CCM board. Due to the assignment of a specific CRC byte for each CCM, the CRC compliance operation is performed in each case. In the event that it matches, the CCM will be activated otherwise it will prevent the data from being sent to the next section. In the first part of the design of the LMP board, it must first be verified that the sent packet is related to which LMP board. Therefore, the first checking is the so called Checksum and then verifying compliance with the address of the Dipswitches and the strap board numbers and CRC will ensure that the data is sent to the correct address. Ensuring the address means activating the Dipswitches in that section. At this stage it is allowed to send commands to the LMP. After allowing the data transmit to the LMP board, it will be examined in detail that which signal lights and which items are considered according to the codes that are assigned to them.

If the command is sent to the red LED signal, the Mains Supply Stop is activated. Also the Mains Supply Proceed is activated for proceed aspects on the LMP and then allowed to check type of signal light and the time of on or off then it activates outputs. In the event that orders sent, but the signal light is not activated in the output section, it will mean an error occurring in this section, which will initially be sent to the CCM board and then sent to the Central Interlocking System as an alert. The data that is presented in Figure 5 is related to the Farhangsara station. It includes the first cabinet, the first sub-rack, LMP1, and the SSA signal light. The transmission order consists of turning on the green aspect for 9 seconds.

4.1. Model in the Loop Simulation

The model in the loop (MIL) is the same as the regular Simulink simulation, with the difference that the separate block is assigned to the controller. Its diagram and simulation in the Simulink environment is presented in Figures 6&7, respectively. Note that the return feedback in this configuration is the same as the monitoring alarms transmitted to the LMP board, then into the CCM board and from there into the interlocking system. This is because the LMP board is not related to the central interlocking unit directly.

After determining the blocks and connecting them to each other, real time RTWT simulator is used, and the corresponding settings are made. The simulation and review of the results in real time are then surveyed. By executing different commands in MIL; its correct and proper operation in real time space is ensured. In this simulation, the duration of each green and red aspects is 9 seconds. The duration of the yellow aspect is 2 seconds, which is actually the changeover between the red and green aspects. The duration of the signal “staying on” is altered according to the interlocking logic that is used by

the user, and the occupancy and free movement of the tracks can be altered.

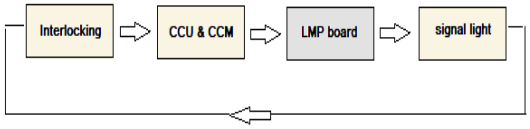

Figure 6. Model in the loop diagram

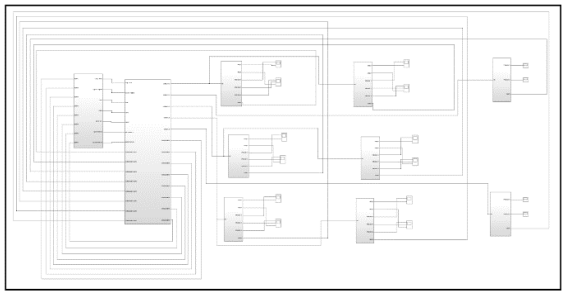

Figure 7. Model in the loop simulation

The commands, such as the standard loop setting, the address of the Dip switches of each section and the straps, the type of signal and the type of aspect that is supposed to execute the commands, the signal lights off or on, as well as the duration of the execution of the command, is modeled in this section. Based on the designated headway of 3 minutes for Tehran subway, and taking only one train on the route, orders are sent to the desired location.

4.2. Hardware in the Loop Simulation

In this section, the LMP board, the hardware and the interlocking unit, the CCM board, and the signal lights are simulated as in real-time. Therefore, the designed LMP board in compiled on the Arduino board and the corresponding connections to the loop closure are provided by RS-232 serial communication. The model for the hardware in the loop simulation in the Simulink environment and the corresponding flow diagram are presented in Figures 8&9, respectively. The configuration of the data sent by the hardware of the Arduino board to the signal lights includes green and yellow proceed aspect and the red stop aspect, Figure 10. Note that the DW signal light is a component of the proceed aspect.

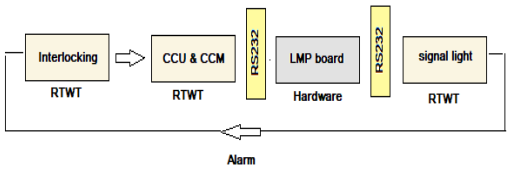

Figure 8. The hardware in the loop diagram

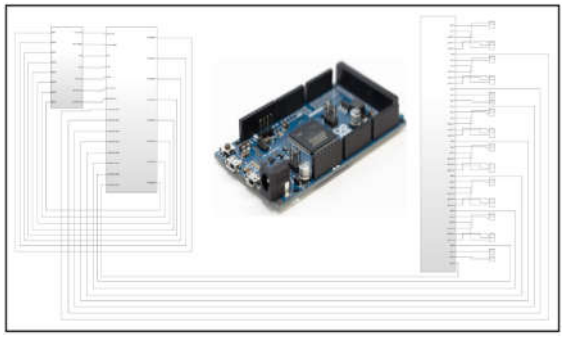

Figure 9. The hardware in the loop simulation

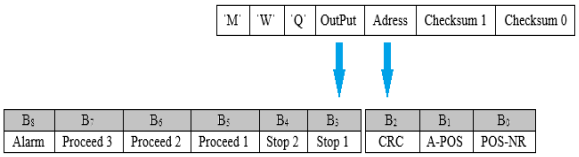

Figure 10. Configure serial communication commands sent to signal light from LMP

In the design section for signal lights, a block called a telemetry is inserted. This block actually examines the data packets sent by RS-232 communication to the display section. This operation is used to monitor and identify the data received from the Arduino board, to determine which signal lights and which displays should be turned on and for how long. The received signal may be delayed, which means that the storage location of the data on a computer named FIFO (First Input First Output) is filled in and there is a time interval between the data being spilled on the FIFO until it is removed. Therefore, the Do-while loop needs to be used to correct it. In fact, the Do-while loop executes the blocks inside it as long as the conditions are ok. Consider the length of the packet as a loop condition. If the length of the data packet is complete, the data is removed, which means emptying the FIFO. With the Show Data Ready port option in the data packet block, it can be checked if the data is present in FIFO or not. In fact, in this section, creation of delay over the sampling time at each stage of the data transfer to the Arduino board and its leak into the software display is prevented.

However, due to the asynchronous nature of the serial communication both the sending and receiving delay time is equal to 0.02 seconds, and in general, the output signal of the signal light in the HIL is 0.04 seconds. As known, this is not in conflict with the real time. To compare the simulations of the MIL and the HIL, green aspect of SSA signal light in the first cabinet of

the OC system of the Farhangsara station is considered. Note that sending and receiving data in HIL simulation latency is twice the sampling time. To detect whether this delay is due to the normalization phase of the software phase or the compiled part on the hardware, the delay block is used. In fact, at this stage, it is examined if there is a difference in the output of the two simulations. If there are differences are they due to the defect of the hardware and the code running on it, or is it related to the real time execution. Then by using the delay block as far as possible, it is intended to push these two simulations to approach each other in terms of performance. In the situation where placing the delay block matches the results of both simulations, it indicates the controller's accuracy, which includes LMP board. Because of the optimal use of the available bandwidth, each section sends commands and addresses using quantum code that is assigned to it. The error caused by changing the data format when sending and receiving is calculated and is presented in Figure 11. The estimated error in simulation is within the range of [1,0], which is an acceptable level compared to 220V output of LMP board.

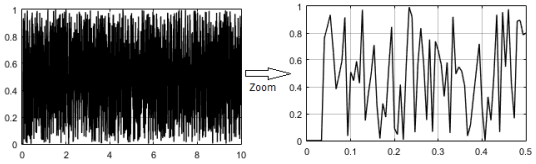

Figure 11. Error in the output voltage of the LMP board

Assuming that when transmitting data, the disturbance with a frequency of 0.01 Hz and range of 0.1 to the output voltage is superimposed, the voltage overflows at a cross section of 220 volts. A solution to prevent loss of data in this situation is to put saturation before the quantification gate. When the signal is increased from saturation, it will be cut at that point, and will not allow overflow and loss of data. The results that are calculated and are presented in Figures 12, 13 and 14 indicate the validity of this statement. In order to evaluate the accuracy of the LMP board and HIL test, input and output signal commands in the hardware of the loop are compared with the main table of signal ranges and are presented in Table 2. Table 3 also presents the results of the signals in HIL.

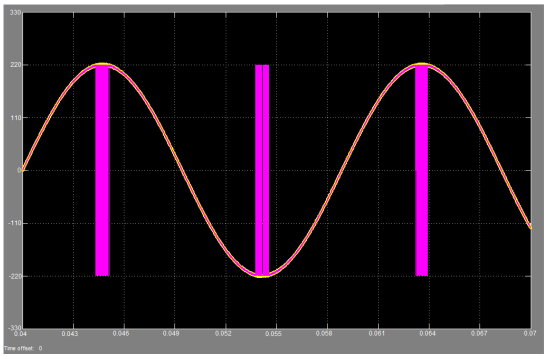

Figure 12. Disturbance effect on the output of the LMP

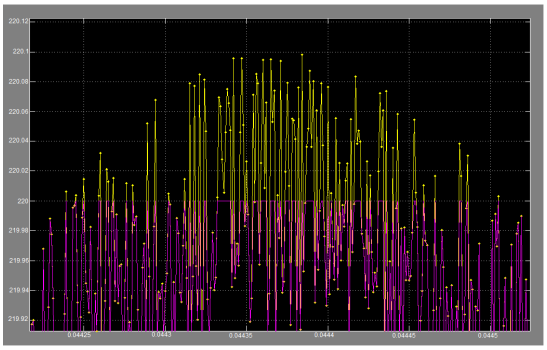

Figure 13. The results with the disturbance and saturation

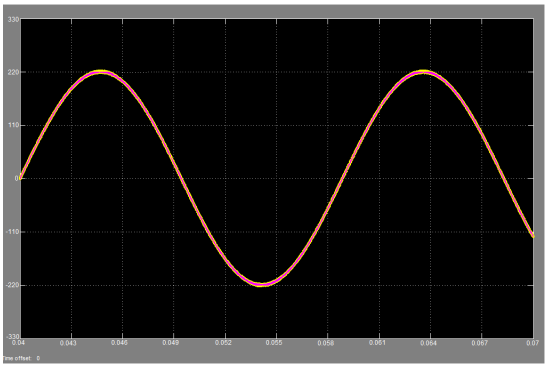

Figure 14. The results with the disturbance and saturation

The inputs and outputs of the simulator have certain numerical ranges and are more accurate than the inputs and outputs of the real system due to the quantification of the data and the change of the data format when sending commands.

5. Conclusions

In this research, the design of a hardware in the loop test structure on the signal light of the LMP board of object controller system located at Farhangsara station in Tehran subway Line 2 was investigated. The complete introduction of the

object controller system and the way of communications between the system with the interlocking system and wayside equipment, and the evaluation of the performance of the LMP and CCM boards were examined.

Table 2. Signal list of real system

Signal list for the Object controller system					
Subsystem	I/O	Range (V)	Sample Rate (HZ)	Resolution (Units)	Power
CCM	Input	5±3%	50±5%	0.15 V	
CCM	RS232*	———	50±5%	———	———
LMP	RS232*	———	50±5%	———	———
LMP	Input	110±3%	50±5%	3.3 V	
LMP	Input	110±3%	50±5%	3.3 V	
LMP	Input	28±3%	50±5%	0.84 V	
LMP	Input	0±3%	50±5%		
LMP	Output	220±3%	50±5%	6.6 V	
LMP	Output	220±3%	50±5%	6.6 V	
LMP	Output	220±3%	50±5%	6.6 V	
LMP	Output	220±3%	50±5%	6.6 V	
LMP	Output	220±3%	50±5%	6.6 V	
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5

Table 3. Signal list of the HIL test

Signal list for the Object controller system					
Subsystem	I/O	Range (V)	Sample Rate (HZ)	Resolution (Units)	Power
CCM	Input	6±3%	50±5%	0.18 V	
LMP	Input	112±3%	50±5%	3.36 V	
LMP	Input	112±3%	50±5%	3.36 V	
LMP	Input	28.5±3%	50±5%	0.855 V	
LMP	Input	0.2±3%	50±5%	0.006V	
LMP	Output	221±3%	50±5%	6.63 V	
LMP	Output	221±3%	50±5%	6.63 V	
LMP	Output	221±3%	50±5%	6.63 V	
LMP	Output	221±3%	50±5%	6.63 V	
LMP	Output	221±3%	50±5%	6.63 V	
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5
Transformer	Output (or input of signal)	12 – 13 – 14- 16	50±5%		25-27.5

Since due to security reasons, access to the LMP board was not feasible for the study, the board of the relevant section was implemented on the hardware of the Arduino board. How to send commands and addresses and the configuration of the serial communication in the hardware in the loop is explored. To ensure that sending data is correct, the Checksum and CRC byte orders are sent. The results of the hardware in the loop are compared with the design stage of the model in the loop.

Due to the exclusivity of the documentation and information concerned with the object controller to their manufacturing companies, there is not much data publically available to cover many aspects of hardware, software and information exchange between sub-systems. Therefore, there are many questions remaining to be explored through further research. To further understand and evaluate object controllers some suggestions are:

- Examining some other boards in the object controller and related communications.
- Checking the hardware related to LMP board and using it in the hardware in the loop in order to approach its prototype production and to calculate its fault tree and reliability.
- Designing automatic interlocking commands to review all aspects of the subway line fully and simultaneously.
- Designing both LED and bubble signals simultaneously in the test, and sending appropriate feedback to the interlocking system.
- Designing LMP board in such a way as to be redundant in time, by changing the structure of sending and receiving regulatory information.

References

[1] Marco Aurelio, Antonio Sanvido, Hardware-in-the-loop Simulation Framework, Diss. ETH Zurich, (2002).

[2] Ashwin C. Sullia, Development & Evaluation of Traffic Signal Optimization Model with Hardware-in-the-Loop Simulation, M.Sc. Thesis, Utah State University, Logan, Utah, (2005).

[3] F. Addeo, B. Allotta, M. Malvezzi, L. Pugi, A. Tarasconi & M. Violani, ATP/ATC subsystem testing and validation using a HIL test rig, WIT Transactions on the Built Environment 74, (2004).

[4] Clément Mayet, Philippe Delarue, Alain Bouscayrol, Eric Chattot, Hardware-in-the-Loop simulation of traction power supply for power flows analysis of multitrain subway lines, IEEE

Transactions on Vehicular Technology, 66(7), (2017), pp. 5564-5571.

[5] Jon del Olmo, Javier Poza, Fernando Garramiola, Txomin Nieva, Leire Aldasoro, Model driven Hardware-in-the-Loop fault analysis of railway traction systems, (ECMSM), 2017 IEEE International Workshop of Electronics, Control, Measurement, Signals and their Application to Mechatronics, (2017).

[6] B. Allotta, R. Conti n , E. Meli, L. Pugi, A. Ridolf, Development of a HIL railway roller rig model for the traction and braking testing activities under degraded adhesion conditions, International Journal of Non-Linear Mechanics, 57, (2013), pp. 50-64.

[7] R. Conti, E. Meli, A. Ridolfi, A. Rindi, An innovative hardware in the loop architecture for the analysis of railway braking under degraded adhesion conditions through roller-rigs, Mechatronics, 24(2), (2014), pp. 139-150.

[8] Dong-Chan Lee, Chul-Goo. Kang, A mechanical brake hardware-in-the-loop simulation of a railway vehicle that accounts for hysteresis and pneumatic cylinder dynamics, Advances in Mechanical Engineering, 7(11), (2015), DOI: 10.1177/1687814015616086.

[9] Moon K. Kwak, Jae-Ha Lee, Dong-Ho Yang & Won-Hee You, Hardware-in-the-loop simulation experiment for semi-active vibration control of lateral vibrations of railway vehicle by magneto-rheological fluid damper, Vehicle System Dynamics, 52(7), (2014), pp. 891-908.

[10] H. Bolandi, M. Haghparast, M. Abedi, A reliable fault tolerant attitude control system based on an adaptive fault detection and diagnosis algorithm together with a backstepping fault recovery controller, Scientia Iranica, Transaction D, Computer Science & Engineering, Electrical, 20(6), (2013), pp. 1999-2014.

[11] M.R. Maleki, A. Amiri, A.R. Taheriyoun, Identifying the time of step change and drift in phase II monitoring of autocorrelated logistic regression profiles, Scientia Iranica, 25(6), (2018), pp. 3654-3666.

[12] A. Rezaee, B. Zamani, A novel approach to automatic model-based test case generation, Scientia Iranica, Transaction D, Computer Science & Engineering, Electrical, 24(6), (2017), pp. 3132-3147.

[13] B. Manfred, What is the benefit of a model-based design of embedded software systems in the car industry?, Software Design and Development: Concepts, Methodologies, Tools, and Applications, IGI Global, (2014), pp. 310-334.

[14] Bardh Hoxha, Adel Dokhanchi, Georgios Fainekos, Mining parametric temporal logic properties in model-based design for cyber-physical systems, International Journal on Software Tools for Technology Transfer, 20(1) , (2018), pp. 79-93.

[15] Imad Zaza, Paolo Nesi, POR CReO, FESR2007, Report of a comparative analysis of the Interlocking Systems, (2014).

[16] F. Hagelin, General Application Information for OCS950 Object Controller System, (2001).

[17] OCS950 maintenance training, Pakistan railways rehabilitation signaling project.

[18] Suchit Puri, Ember Web Development with Ember CLI, Packt Publishing Ltd., (2015).

[19] G. Teeg, S. Vlasenko, Railway Signaling and Interlocking, International Compendium, DVV Media. Eurailpress 475, (2009).

[20] Pieter J. Mosterman, Automatic code generation: Facilitating new teaching opportunities in engineering education, Frontiers in Education, Conference, 36th Annual. IEEE, (2006).

[21] Dennis M. Buede, William D. Miller, The engineering Design of Systems: Models and Methods, John Wiley & Sons, (2016).

[22] José Carlos Molina Fraticelli, Simulink Code Generation: Tutorial for generating C code from Simulink Models using Simulink Coder, Nasa Marshall Space Flight Center, (2012).

[23] Application Information for Signal Object Controller, Tehran Metro".2000.3NSS002035D0103.